What is claimed is:

1. A method of controlling an output buffer circuit comprising a first drive circuit for receiving an input signal having a sharp waveform and generating an output signal that has a gentle waveform and is output from an output terminal of the output buffer circuit, and a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, the method comprising the steps of:

changing the output signal in accordance with a change in the input signal using the first drive circuit; and

driving the second drive circuit after the output signal is changed by a predetermined amount.

2. A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate an output signal having gentle waveform in response to an input signal having a sharp waveform, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating the output signal in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit in accordance with the control signal.

3. The method according to claim 2, wherein the output signal generating step includes generating the output signal by turning on the first output transistor;

the driving step includes turning on the third output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the first and third output transistors in accordance with a change in the input signal.

4. The method according to claim 2, wherein the output signal generating step includes generating the output signal by turning on the second output transistor;

the driving step includes turning on the fourth output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the second and fourth output transistors in accordance with a change in the input signal.

5. An output buffer circuit comprising:

a first drive circuit for receiving an input signal having a sharp waveform and generating an output signal that has a gentle waveform and is output from an output terminal of the output buffer circuit;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive

circuit;

a delay circuit, connected to the output terminal, for delaying the output signal and generating a delayed output signal; and

a first control circuit, connected between the delay circuit and the second drive circuit, for receiving the input signal and the delayed output signal and generating first control signal for driving the second drive circuit.

6. The output buffer circuit according to claim 5, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate the output signal having the gentle waveform; and

the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors.

7. The output buffer circuit according to claim 6, wherein the first control circuit turns on the third output transistor with the first control signal in response to the delayed output signal after the first output transistor is turned on by the input signal, and the first control circuit turns on the fourth output transistor with the first control signal in response to the delayed output signal after the second output transistor is turned on by the input signal.

8. The output buffer circuit according to claim 6,

further comprising a second control circuit, connected to the first drive circuit, for inverting the input signal to generate second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal that have phases opposite to a phase of the input signal and are respectively supplied to the third and fourth output transistors.

9. The output buffer circuit according to claim 6, further comprising a second control circuit, connected to the first drive circuit, for generating second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal respectively supplied to the third and fourth output transistors.

10. The output buffer circuit according to claim 5, wherein the second drive circuit includes a plurality of sub-drive circuits having different impedances, wherein at least one of the sub-drive circuits is selectively enabled to set the output impedance of the second drive circuit.

11. The output buffer circuit according to claim 10, wherein the first control circuit supplies the first control signal to each of the sub-drive circuits based on the input signal, the delay signal and a select signal.

12. An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, connected to the

first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal at an output terminal of the output buffer circuit; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, wherein the third control circuit controls the first and second control circuits when the first and second output transistors are turned off to generate the first and second control signal in accordance with the input signal, and controls the first and second control circuits when the first and second output transistors are turned on such that the first and second control signals sharply rise or fall in response to a change in the input signal, gently rise or fall after a predetermined time elapses, and thereafter sharply rise or fall when the output signal reaches a predetermined level.

13. The output buffer circuit according to claim 12, wherein the first and second control circuits respectively include first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

the output buffer circuit further comprises a delay circuit, connected to the third control circuit, for generating a delay signal by delaying the input signal,

wherein when the first and second output transistors

are turned on, the third control circuit controls the first and second control circuits in accordance with the delay signal and the output signal such that the first and second control signals are generated by turning on and off the first and second switching elements.

14. The output buffer circuit according to claim 13, wherein the third control circuit includes:

a first inverter circuit, connected to the output terminal and having a relatively low threshold voltage, for receiving the output signal and generating a first inverted signal;

a second inverter circuit, connected to the output terminal and having a relatively high threshold voltage, for receiving the output signal and generating a second inverted signal;

a NAND gate, connected to the delay circuit and the first inverter circuit, for receiving the delay signal and the first inverted signal and generating a first switching control signal for controlling the first switching element; and

a NOR gate, connected to the delay circuit and the second inverter circuit, for receiving the delay signal and the second inverted signal and generating a second switching control signal for controlling the second switching element.

15. The output buffer circuit according to claim 13, wherein the third control circuit includes:

a Schmitt inverter circuit, connected to the output terminal and having a hysteresis characteristic, for receiving the output signal and generating an inverted output signal;

a NAND gate, connected to the delay circuit and the

Schmitt inverter circuit, for receiving the delay signal and the inverted output signal and generating a first switching control signal for controlling the first switching element; and

a NOR gate, connected to the delay circuit and the Schmitt inverter circuit, for receiving the delay signal and the inverted output signal and generating a second switching control signal for controlling the second switching element.

16. An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, respectively connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal that is output from an output terminal of the output buffer circuit in response to the first and second control signals, the first and second control circuits respectively including first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, the third control circuit including,

a first inverter circuit, connected to the output terminal and having a relatively low threshold voltage, for

receiving the output signal and generating a first inverted signal,

a second inverter circuit, connected to the output terminal and having a relatively high threshold voltage, for receiving the output signal and generating a second inverted signal,

a NAND gate, connected to the first inverter circuit, for receiving the input signal and the first inverted signal and generating a first switching control signal for controlling the first switching element, and

a NOR gate, connected to the second inverter circuit, for receiving the input signal and the second inverted signal and generating a second switching control signal for controlling the second switching element.

17. An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, respectively connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal that is output from an output terminal of the output buffer circuit in response to the first and second control signals, the first and second control circuits respectively including first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and

controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, the third control circuit including,

a Schmitt inverter circuit, connected to the output terminal and having a hysteresis characteristic, for receiving the output signal and generating an inverted output signal,

a NAND gate, connected to the Schmitt inverter circuit, for receiving the input signal and the inverted output signal and generating a first switching control signal for controlling the first switching element, and

a NOR gate, connected to the Schmitt inverter circuit, for receiving the input signal and the inverted output signal and generating a second switching control signal for controlling the second switching element.

18. A semiconductor device comprising:

an output buffer circuit including,

first and second output transistors connected in series between a first power supply and a second power supply,

first and second control circuits, connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal output from an output terminal of the output buffer circuit in response to the first and second control signals, and

a third control circuit, respectively connected between the output terminal and the first and second control circuits, for receiving the input signal and the output

signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, wherein the third control circuit controls the first and second control circuits when the first and second output transistors are turned off to generate the first and second control signal in accordance with the input signal, and controls the first and second control circuits when the first and second output transistors are turned on such that the first and second control signals sharply rise or fall in response to a change in the input signal, gently rise or fall after a predetermined time elapses, and thereafter sharply rise or fall when the output signal reaches a predetermined level.